REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated August 9, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due consideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-12 are under consideration in this application. Claims 1-4 and 9 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention.

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-4, 7 and 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,851,440 to Tanaka et al. (hereinafter "Tanaka"), claims 5, 6 and 9-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of US Patent No. 6,887,724 to Namakura et al. (hereinafter "Namakura"), US Patent No. 6,479,837 to Ogawa (hereinafter "Ogawa"), US Patent No. 6,673,639 to Wada et al. (hereinafter "Wada"), US Application No. 2002/0158298 to Yamada et al. (hereinafter "Yamada"), and US Application No. 2002/0142567 to Hagino et al. (hereinafter "Hagino"), and claim 12 was rejected as being unpatentable over Tanaka in view of Namakura, Ogawa, Hagino, Wada and US Application No. 2004/0038438 to Shih et al. (hereinafter "Shih"). These rejections have been carefully considered, but are most respectfully traversed.

The image display device of the invention provided with an active-matrix substrate (for example, the embodiment depicted in Fig. 6, pp. 16-17), as now recited in claim 1, comprises: an insulating substrate INS; and a plurality of circuit regions fabricated on said insulating substrate INS and including at least a pixel section and a pixel-driving circuit section, each of said pixel section and said pixel-driving circuit section having a polycrystalline silicon semiconductor film PSI. At least one of said plurality of circuit regions

has a first type of a thin film transistor SWTR1 and a second type of a thin film transistor SWTR2. An angular orientation of a direction of a current flowing through a channel of said first type of a thin film transistor SWTR1 is *formed to be **non-parallel** with* an angular orientation of a direction of a current flowing through a channel of said second type of a thin film transistor SWTR2.

For example, a switch SW (Fig. 6) is provided in each pixel and formed of thin film transistors for retaining, discharging and storing charges. The elements constituting the pixel PXL are fabricated from the polycrystalline silicon film PSI converted from amorphous silicon by using excimer laser as explained in connection with FIGS. 3A(1) to 3A(2). No anisotropy is present in the polycrystalline silicon film PSI of FIGS. 3A(1) to 3B(2) and therefore, regardless of what the orientation of the layout of a thin film transistor is, there is little difference in characteristics of the thin film transistor. The switch SW of FIG. 6 has a double-gate structure comprised of two thin film transistors SWTR1 and SWTR2 so as to improve withstand voltages (p. 16, line 19 to p. 17, line 11). In this example, for the purpose of reducing an area of the layout of the two thin film transistors and improving the aperture ratio of the pixel, the angular orientation for aligning the source region and drain region of the thin film transistor SWTR1 is perpendicular to the angular orientation for aligning the source region and drain region of the thin film transistor SWTR2 in the layout as shown in FIG. 6. Another similar configuration in accordance with the present invention is also illustrated as the region RGN1 in FIG. 12 .

The invention (for example, the embodiment depicted in Fig. 1) recited in claim 2 is directed to a plurality of circuit regions includes at least one pair of a first circuit region and a second circuit region, all thin film transistors in said first circuit region flow currents through channels thereof in a first angular orientation, all thin film transistors in said second circuit region flow currents through channels thereof in a second angular orientation, and said first angular orientation is *formed to be **non-parallel** with* said second angular orientation.

For example, in FIG. 1 of the present application, while all the TFTs in the shift register DSR are arranged to flow currents in an angular orientation parallel with the long sides of the glass substrate SUB, all the TFTs in the sampling switches SSW are arranged to flow currents in an angular orientation perpendicular to the long sides of the glass substrate SUB.

In contrast, the angular orientations of channel directions of Tanaka's bipolar TFT T1 and monopolar TFT T2 (Fig. 1) are *formed to be **parallel*** (rather than "non-parallel") *with*

each other (S -> D vs. D <- S). The current direction through the bipolar TFT T1 can be made either identical with or opposite to the current direction through the monopolar TFT T2 (Figs. 9-10).

The image display device of the invention provided with an active-matrix substrate, as now recited in claim 9, has a plurality of circuit regions fabricated on one insulating substrate INS and including at least a pixel section and a pixel-driving circuit section, each of said pixel section and said pixel-driving circuit section having thin film transistors TFTs formed of polycrystalline silicon films PSI. (1) In said polycrystalline silicon films in a channel, a source region and a drain region of said thin film transistors constituting said pixel section, (i) an average crystalline grain diameter is 1 μm or smaller, and (ii) a peak-to-valley height difference of a surface is equal to or greater than 20 nm. While (2) in at least one of said plurality of circuit regions excluding said pixel section, (i) crystalline grains of said polycrystalline silicon films are of a rectangular shape of 0.3 μm to 2 μm in width and 4 μm or more in length in a channel, a source region and a drain region of said thin film transistors, and (ii) a peak-to-valley height difference of a surface of said channel, said source region and said drain region of said thin film transistors is equal to or smaller than 5 nm.

First, Applicants respectfully point out the claim 9 does not define directions of currents as claims 1-2. The current direction discussion on page 6, last paragraph of the outstanding Office Action was irrelevant.

Second, contrary to the Examiner's allegation (p. 7, last 2 lines and p. 8, lines 1-6 of the outstanding Office Action), applicants respectfully contend that a person of ordinary skill would not be motivated to either modify or combine the cited references in such a manner as to embody each and every feature of the present invention as now claimed. Applicants further contend that the combination of references used by the Examiner merely consists of selecting bits and pieces from each reference, and then combining those bits and pieces using knowledge or hindsight gleaned from the disclosure of the present invention as a guide to support the combination. The well established rule of law is that each prior art reference must be evaluated in its entirety, and that all of the prior art must be considered as a whole," *Panduit Corp. v. Dennison Mfg. Co.*, 227 USPQ 337, 344 (Fed. Cir. 1985). See *Para-Ordinance Mfg, Inc. v. SGS Importers Intl.*, Inc., 73 F.3d 1085, 37 USPQ2d 1237 (Fed. Cir. 1995) ("Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor.").

Third, the invention recited in claim 9 varies characteristics for TFTs in respective circuit regions depending upon the functions of the respective circuit regions (e.g., different blocks in Fig. 2) such that the characteristics of polycrystalline silicon films are made different in respective circuit regions. In particular, the pixel section requires performance of higher breakdown voltages and lower leakage currents such that an average crystalline grain diameter ≤ 1 μm, and a peak-to-valley height difference ≥ 20 nm are provided. On the other hand, other circuit regions require larger crystalline grains (a rectangular shape of 0.3-2 μm wide and ≥ 4 μm long) and a smaller peak-to-valley height difference ($\leq$5 nm).

A mere combination of the polycrystalline silicon films disclosed by Nakamura, Ogawa and Wada will not achieve TFTs having the high-breakdown-voltage, low-leakage performance disclosed by the present application. Although Yamada's TFTs with a polycrystalline silicon layer with large grain sizes improves switching speed suitable for driver circuitry, and Hagino's transistor with a semiconductor layer having a peak-to-peak height difference of 60 nm provides high smoothness and highly reliability, neither Yamada nor Hagino teach "varying performance of TFTs in different circuit regions by changing the physical characteristics of the TFTs in a pixel region with respect to other circuit regions formed of polycrystalline silicon films PSI on one insulating substrate INS". Even if, arguendo, a person of ordinary skill were motivated to combine the references as suggested by the Examiner, such combined teachings would still fall short in fully meeting the Applicants' claimed invention as set forth in claim 9.

Neither Tanaka, Namakura, Ogawa, Wada, Yamada, Hagino, and Shih, nor their combinations teaches or suggests each and every feature of the present invention as recited in independent claims 1-2 and 9, from which other claims depend. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor

rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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